

FIG. 1
PRIOR ART

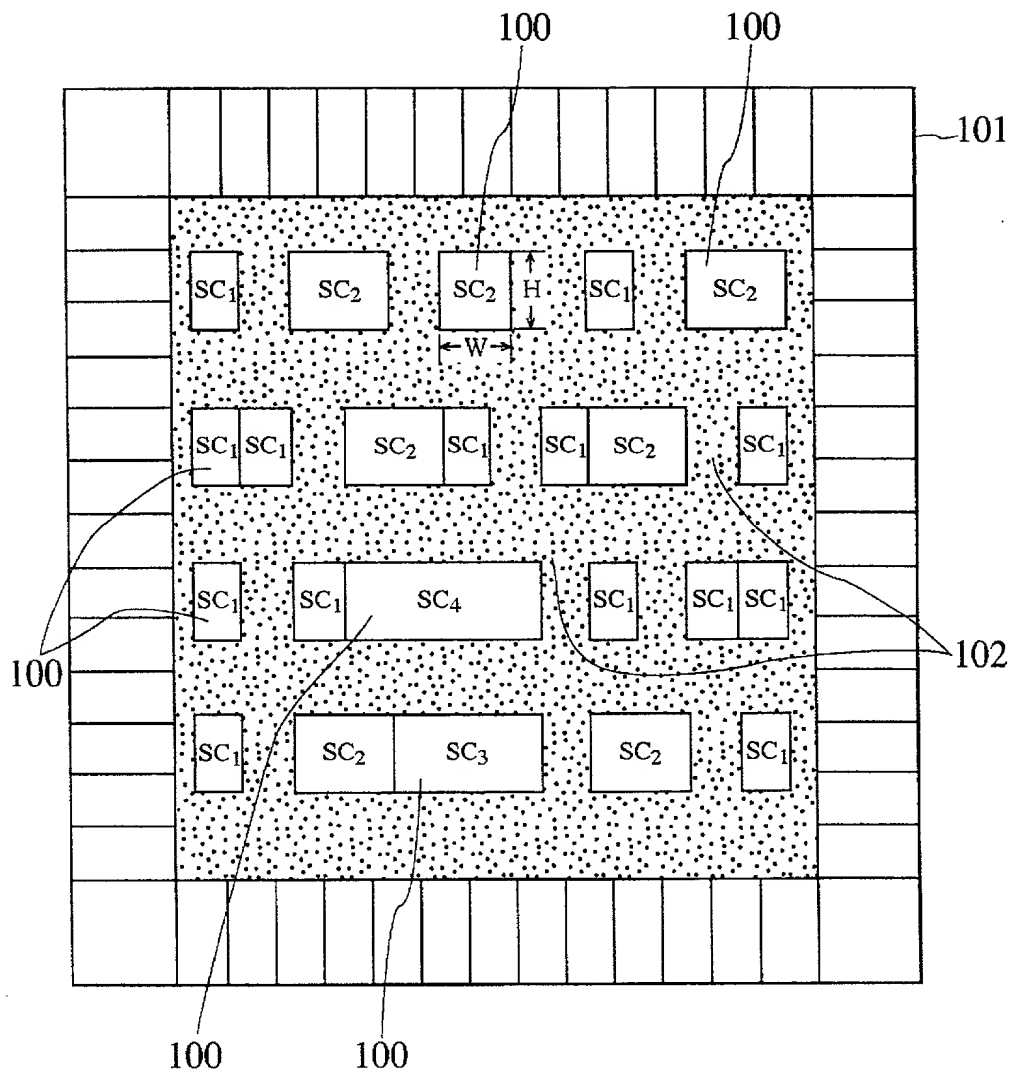


FIG. 2
PRIOR ART

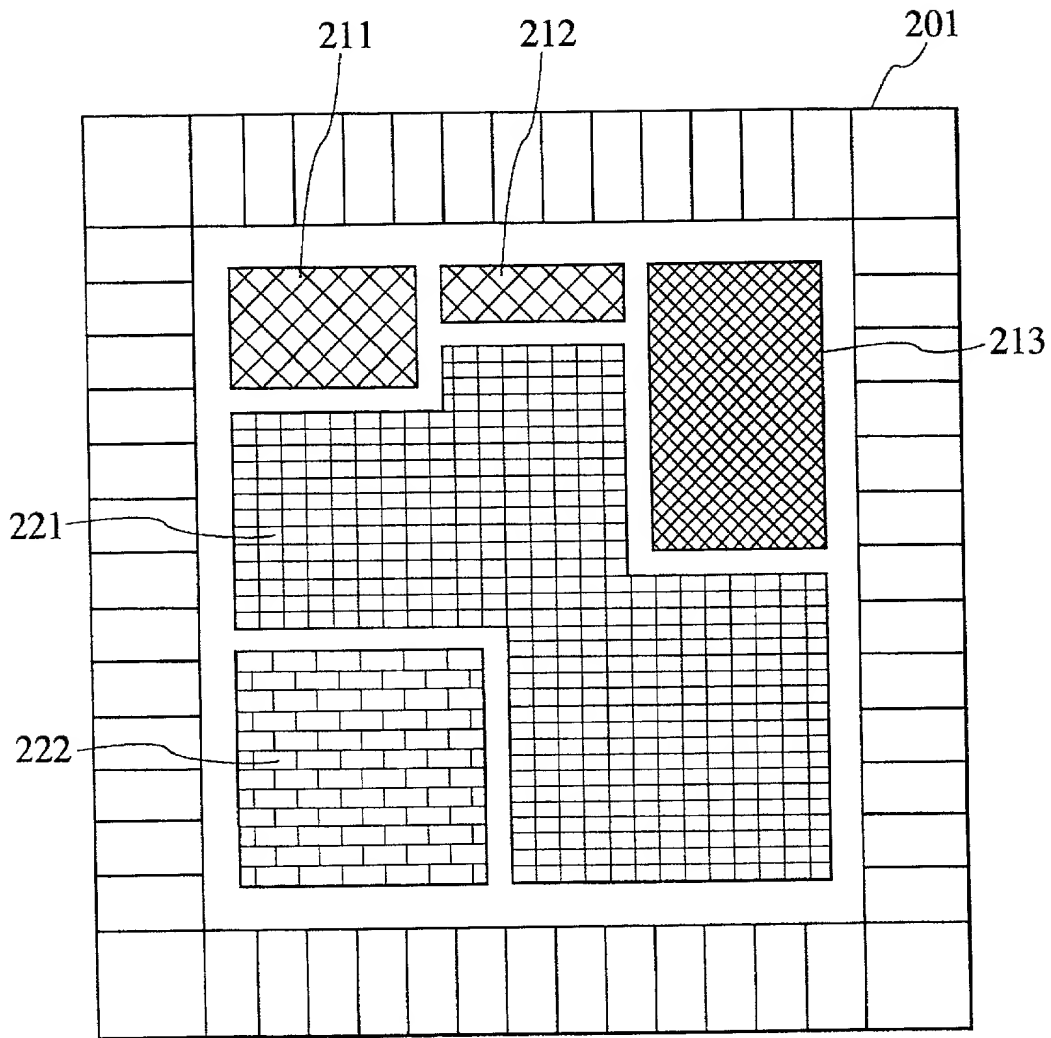


FIG. 3A

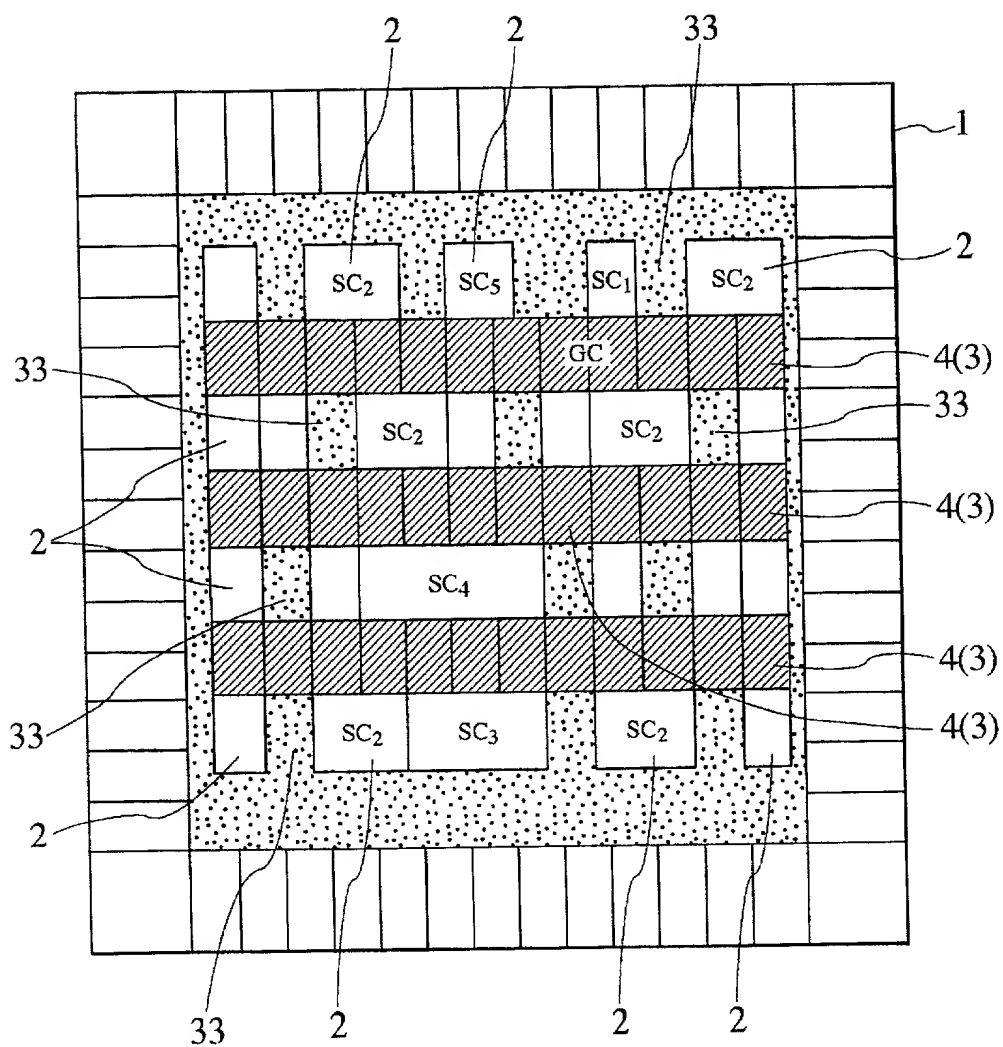


FIG. 3B

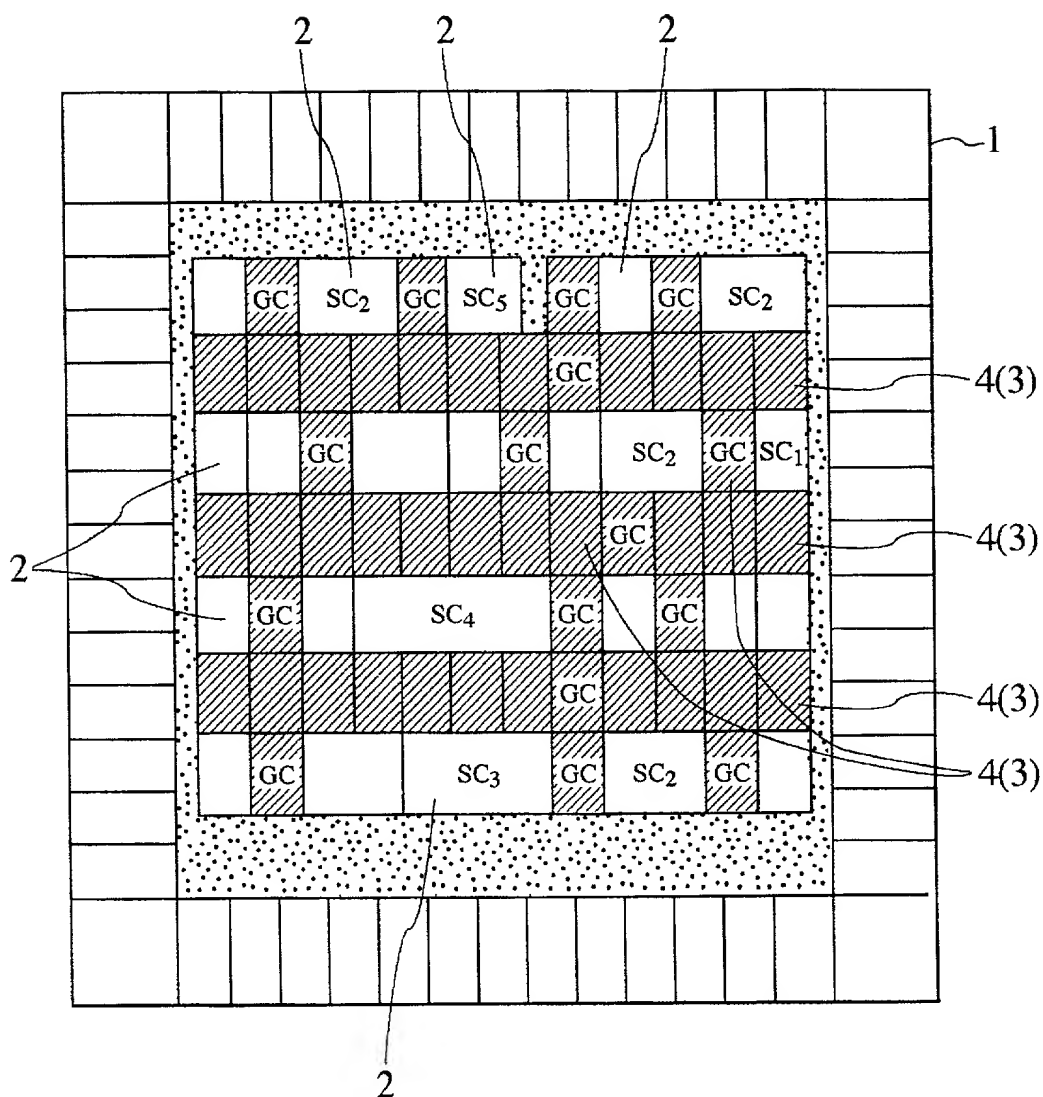


FIG. 3C

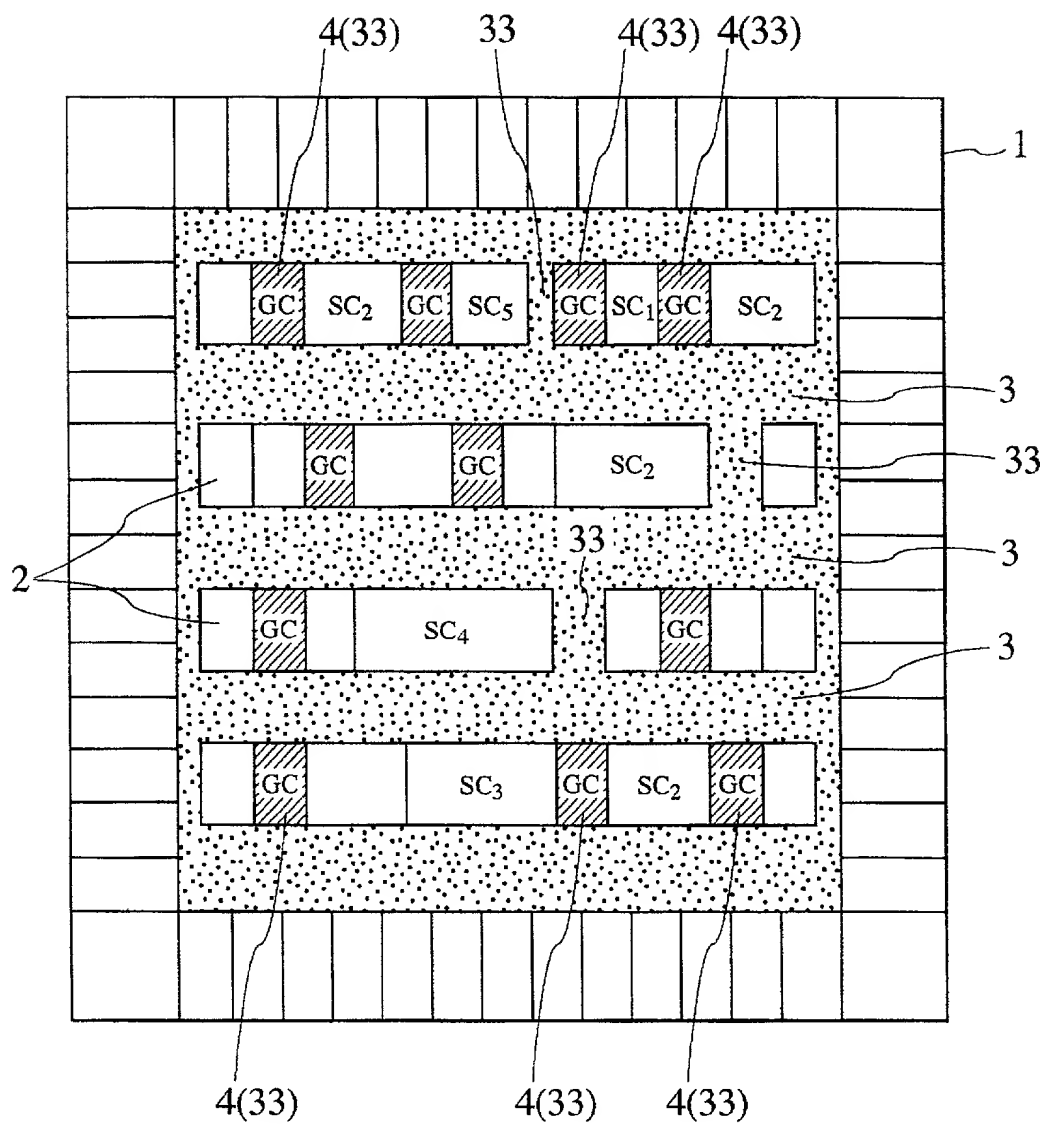
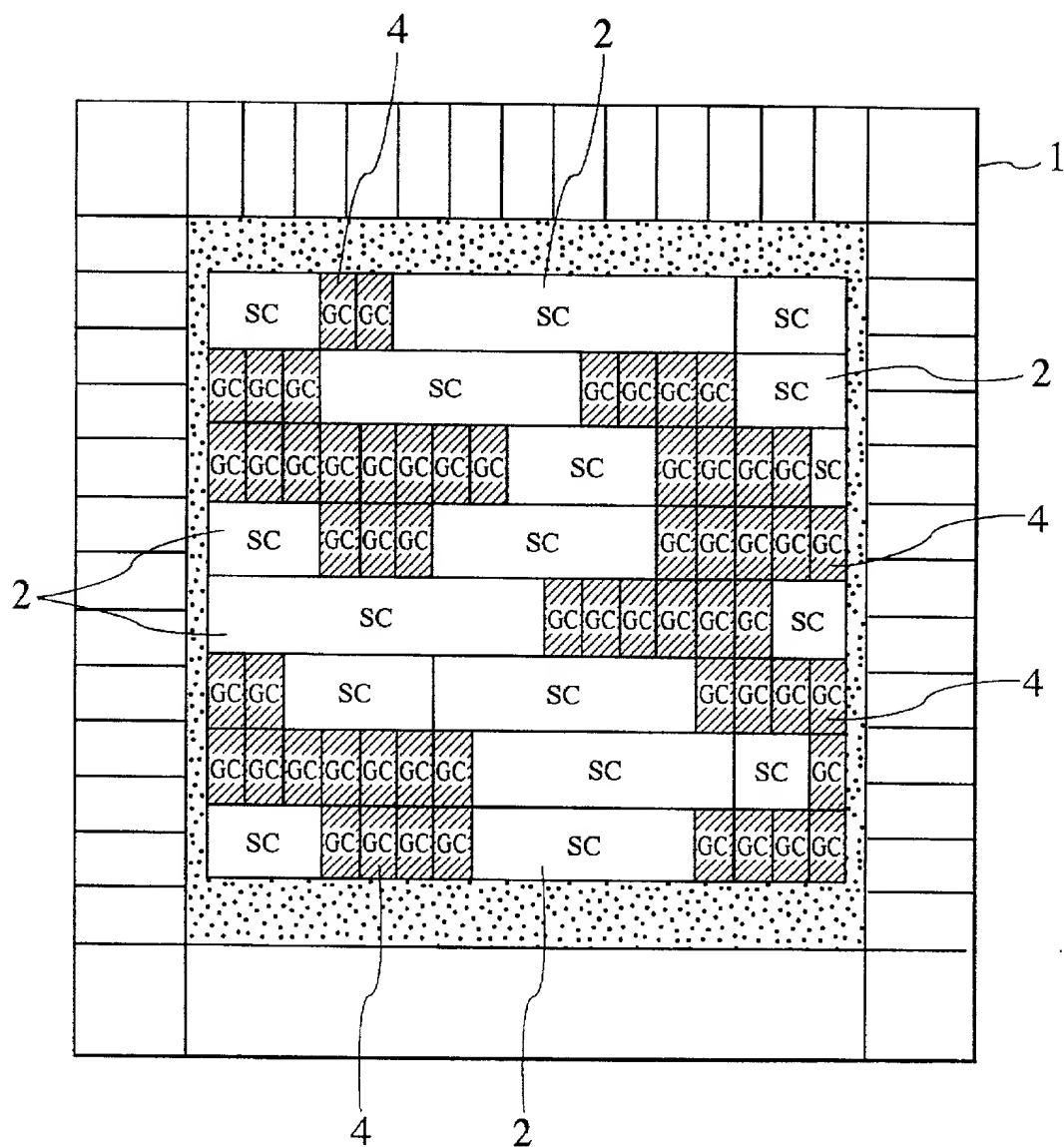


FIG. 3D



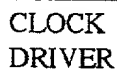
[illegible]

Figure 1 is a schematic diagram of a memory array. The array is a grid of cells. A 'CLOCK DRIVER' is connected to a vertical line (labeled 2) that runs through the center of the array. Two shaded rectangular cells are labeled 4. The top and bottom rows of the array are labeled 1. The left and right columns of the array are labeled 2.

CLOCK DRIVER